LISTING OF THE CLAIMS

This listing of claims replaces all prior versions and listing of claims in the present application:

Claims 1-47 (Canceled)

Claim 48 (Currently amended): ~~The semiconductor device according to claim 46, wherein~~

A semiconductor device comprising a semiconductor substrate, a transistor formed on a surface area of said semiconductor substrate, and a multi-layered interconnection structure including a plurality of interlevel dielectric films and a plurality of interconnect layers overlying said transistor, wherein a high-permeability region is provided in an interlevel dielectric film, wherein:

said high-permeability region includes therein a plurality of high-permeability magnetic rods including a high-permeability material embedded in respective film openings, said film openings having an aspect ratio (depth/diameter or a side) of 1 or above and penetrating at least one of said interlevel dielectric films to reach another of said interlevel dielectric films,

said high-permeability material is a composite material including a low-permittivity insulating material and a high-permeability magnetic material including an electric conductivity or an insulating property.

Claim 49 (Previously presented): The semiconductor device according to claim 48, wherein said low-permittivity insulating material is a porous insulating material.

Claims 50-60 (Canceled)

Claim 61 (Currently amended): ~~The semiconductor device according to claim 58, wherein said on-chip antenna interconnect~~

A semiconductor device comprising a semiconductor substrate having therein a low-capacitance substrate region, a transistor formed on a surface area of said semiconductor substrate, and a multi-layered interconnection structure including a plurality of interlevel dielectric films and a plurality of interconnect layers overlying said transistor, wherein:

a plurality of substrate openings are formed in said low-capacitance substrate region, penetrating at least an undermost one of said interlevel dielectric films to reach an internal of said semiconductor substrate,

an on-chip antenna interconnect is formed on said low-capacitance substrate region and is configured by interconnect layers embedded in slit-like openings which are formed to penetrate a plurality of said interlevel dielectric films.

Claim 62 (Currently amended): ~~The semiconductor device according to claim 59, wherein~~

A semiconductor device comprising a semiconductor substrate having therein a low-capacitance substrate region, a transistor formed on a surface area of said semiconductor substrate, and a multi-layered interconnection structure including a plurality of interlevel dielectric films and a plurality of interconnect layers overlying said transistor, wherein:

a plurality of substrate openings are formed in said low-capacitance substrate region, penetrating at least an undermost one of said interlevel dielectric films to reach an internal of said semiconductor substrate,

an on-chip antenna interconnect is formed on said low-capacitance substrate region in a peripheral area of a semiconductor chip, and

a grounded shield interconnect is formed inside said on-chip antenna interconnect.

Claim 63 (Previously presented): The semiconductor device according to claim 62, wherein said shield interconnect is configured by interconnect layers embedded in slit-like openings formed to penetrate a plurality of said interlevel dielectric films.

Claims 64-77 (Canceled)